CLAIMS

1. A photodetector having a photosensitive region in which pixels are arranged in a two-dimensional array,

wherein each pixel is constructed of a plurality of photosensitive portions each of which outputs an electric current according to an intensity of incident light and which are arranged adjacent to each other within an identical plane,

wherein across a plurality of pixels arrayed in a first direction in the two-dimensional array, photosensitive portions on one side out of the plurality of photosensitive portions forming each of said pixels are electrically connected to each other,

wherein across a plurality of pixels arrayed in a second direction in the two-dimensional array, photosensitive portions on another side out of the plurality of photosensitive portions forming each of said pixels are electrically connected to each other,

the photodetector comprising a signal processing circuit for reading electric currents from groups of photosensitive portions on the one side electrically connected among the plurality of pixels arrayed in the first direction and electric currents from groups of photosensitive portions on the another side electrically connected among the plurality of pixels arrayed in the second direction, and for detecting luminance profiles in the first direction and in the second direction in the two-dimensional array on the basis of the electric currents.

2. The photodetector according to Claim 1, wherein the signal processing circuit comprises:

a shift register for sequentially reading the electric currents from

the groups of photosensitive portions on the one side, in the second direction and for sequentially reading the electric currents from the groups of photosensitive portions on the another side, in the first direction; and

an integrating circuit for sequentially importing the electric currents from the groups of photosensitive portions on the one side and the electric currents from the groups of photosensitive portions on the another side sequentially read by the shift register, and for converting the electric currents into voltages.

3. The photodetector according to Claim 1, wherein the signal processing circuit comprises:

integrating circuits provided corresponding to the groups of photosensitive portions on the one side and the groups of photosensitive portions on the another side, each of which converts either of an electric current from a corresponding group of photosensitive portions on the one side and an electric current from a corresponding group of photosensitive portions on the another side, into a voltage, and outputs the voltage;

CDS circuits provided corresponding to the integrating circuits, each of which outputs a voltage according to a variation amount of the voltage outputted from a corresponding integrating circuit;

sample-and-hold circuits provided corresponding to the CDS circuits, each of which holds a voltage outputted from a corresponding CDS circuit and outputs the voltage; and

a maximum detecting circuit for detecting a maximum of voltages outputted from the respective sample-and-hold circuits; and

an A/D converter circuit for sequentially importing the voltages outputted from the respective sample-and-hold circuits, converting the voltages into digital values on the basis of the maximum detected by the maximum detecting circuit, and outputting the digital values.

4. A photodetector having a photosensitive region,

wherein the photosensitive region comprises a plurality of first photosensitive portions electrically connected to each other in a first direction and a plurality of second photosensitive portions electrically connected in a second direction intersecting with the first direction,

wherein the plurality of first photosensitive portions and the plurality of second photosensitive portions are arrayed in a two-dimensionally mixed state within an identical plane, and

the photodetector comprising a signal processing circuit for reading electric currents from groups of first photosensitive portions electrically connected to each other in the first direction and electric currents from groups of second photosensitive portions electrically connected to each other in the second direction, and for detecting luminance profiles in the first direction and in the second direction in the two-dimensional array on the basis of the electric currents.

5. The photodetector according to Claim 4, wherein the signal processing circuit comprises:

a shift register for sequentially reading the electric currents from the groups of first photosensitive portions in the second direction and for sequentially reading the electric currents from the groups of second photosensitive portions in the first direction; and

an integrating circuit for sequentially importing the electric

currents from the respective groups of first photosensitive portions and the electric currents from the respective groups of second photosensitive portions sequentially read by the shift register, and for converting the electric currents into voltages.

6. The photodetector according to Claim 4, wherein the signal processing circuit comprises:

integrating circuits provided corresponding to the groups of first photosensitive portions and the groups of second photosensitive portions, each of which converts either of an electric current from a corresponding group of first photosensitive portions and an electric current from a corresponding group of second photosensitive portions, into a voltage, and outputs a voltage;

CDS circuits provided corresponding to the integrating circuits, each of which outputs a voltage according to a variation amount of the voltage outputted from a corresponding integrating circuit;

sample-and-hold circuits provided corresponding to the CDS circuits, each of which holds a voltage outputted from a corresponding CDS circuit and outputs the voltage;

a maximum detecting circuit for detecting a maximum of voltages outputted from the respective sample-and-hold circuits; and

an A/D converter circuit for sequentially importing the voltages outputted from the respective sample-and-hold circuits, converting the voltages into digital values on the basis of the maximum detected by the maximum detecting circuit, and outputting the digital values.